REMARKS

The Examiner and his supervisor are thanked for the interview courteously granted to the undersigned, in connection with the above-identified application. During this interview, both the rejection under the second paragraph of 35 USC 112, and the prior art rejection, were discussed. Proposed amended claims 1 and 2, and new claim 9, were provided to the Examiner and his supervisor, and were discussed during this interview. In particular, during the interview it was emphasized that the rejection under the second paragraph of 35 USC 112 was improper, in that the term "gate insulating film" is a term known in the art. In addition, attention was directed to page 1 of Applicants' specification, describing gate oxide films (insulating films), and page 14 thereof.

With respect to the prior art rejections, during the interview the undersigned pointed to proposed amendments to the claims emphasizing that the treatment chamber used in the method of the present claims is a vertical wafer heat treatment chamber of a batch processing vertical oxidation furnace, as compared with the horizontal heat treatment chamber in the applied reference to Ohmi, U.S. Patent No. 5,840,368. In addition, it was pointed out by the undersigned that, as proposed to be amended, the claims recite introduction of the wet oxidative atmosphere into the vertical wafer heat treatment chamber and flow therethrough, which would have neither been disclosed nor would have been suggested from the flow of the gasses from one end to the other end of the oxidation furnace in Ohmi. No specific agreements were achieved during the interview.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention, in light of amendments set forth in the claims as discussed during the aforementioned interview. Specifically, Applicants

have amended claim 1 to recite that the moisture is transferred into a "vertical" wafer heat treatment chamber of a batch processing vertical oxidation furnace "through a gas introducing tube"; and to recite that the wet oxidative atmosphere is introduced into the vertical wafer heat treatment chamber through the gas introducing tube disposed along a wall surface of the vertical wafer heat treatment chamber from its lower end to upper end, and the gas introducing tube has its outlet at the upper end of the vertical wafer heat treatment chamber so that the wet oxidative atmosphere flows from the upper end to the lower end in the vertical heat treatment chamber. In addition, Applicants have amended claim 2 to recite that the thermal oxidation forms an insulating film, thereby providing antecedent basis for "said insulating film" which is a gate insulating film of an insulated gate field effect transistor as also recited in claim 2.

In addition, Applicants are adding new claim 9 to the application. Claim 9, dependent on claim 1, recites that the gas introducing tube is integrally formed with the wall surface of the vertical wafer heat treatment chamber on the wall surface of the vertical wafer heat treatment chamber.

In connection with the amendments to the previously considered claims, and also in connection with the newly added claims, note, for example, pages 1, 14, 68, 72 and 73 of Applicants' specification, especially together with Fig. 30 of Applicants' original disclosure.

Applicants respectfully traverse the rejection of claims 2-4 under the second paragraph of 35 USC 112, as set forth on page 2 of the Office Action mailed June 15, 2005. Contrary to the conclusion by the Examiner, it is respectfully submitted that the term "gate insulating film" is a definite term in the art, especially in light of the description in Applicants' specification, such that the term is not confusing

and unclear in scope. Thus, as set forth in the second paragraph on page 1 of Applicants' specification, it is described that the present invention relates to a method for formation of gate oxide films (insulating films) such as of MOSFET (Metal Oxide Semiconductor Field Effect Transistor). Note also page 14, lines 14-16, of Applicants' specification, describing that in the method for fabricating a semiconductor integrated circuit device, the oxide film comprises a gate oxide film of an MOSFET. See also the enclosed page 83 of Modern Semiconductor Device Physics (1998), edited by S. M. Sze, referring to a "gate insulator" in sections 2.1.1 and 2.1.2. It is respectfully submitted that the Examiner errs in contending that the term "gate insulating film" is confusing and not clear.

In addition, note that claim 2 has been amended to recite that the thermal oxidation forms an insulating film on the silicon member, thus providing antecedent basis for the further recitation in claim 2 that "said insulating film" is a gate insulating film of an insulated gate field effect transistor. Clearly, the metes and bounds of claims 2-4 are sufficiently set forth such that one of ordinary skill in the art would have known whether a specific method fell within or outside the present claims, with respect to the structure formed by the thermal oxidation. It is respectfully submitted that, under the present circumstances, the second paragraph of 35 USC 112 requires nothing more. See In re Moore, 169 USPQ 236 (CCPA 1971).

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the prior art applied by the Examiner in rejecting claims in the Office Action mailed June 15, 2005, that is, the teachings of the U.S. patent to Ohmi, No. 5,840,368, under the provisions of 35 USC 102 and 35 USC 103.

It is respectfully submitted that the reference as applied by the Examiner would have neither taught nor would have suggested such method for fabricating a semiconductor integrated circuit device as in the present claims, including wherein the moisture, prepared using a catalyst, is transferred into a vertical wafer heat treatment chamber of a batch processing vertical oxidation furnace through a gas introducing tube to form a wet oxidative atmosphere, the wet oxidative atmosphere being introduced into the vertical wafer heat treatment chamber through the gas introducing tube disposed along a wall surface of the vertical wafer heat treatment chamber from its lower end to upper end, with the gas introducing tube having its outlet at the upper end of the vertical wafer heat treatment chamber so that the wet oxidative atmosphere flows from the upper end to the lower end in the vertical heat treatment chamber. See claim 1.

In addition, it is respectfully submitted that the applied reference would have neither taught nor would have suggested such method, utilizing the vertical wafer heat treatment chamber with flow of wet oxidative atmosphere as discussed previously in connection with claim 1, and, additionally, wherein the gas introducing tube is integrally formed with the wall surface of the vertical wafer heat treatment chamber, on the wall surface of the vertical wafer heat treatment chamber. See claim 9.

Moreover, it is respectfully submitted that the teachings of the applied reference would have neither disclosed nor would have suggested such method for fabricating a semiconductor integrated circuit device, as discussed previously, and wherein the thermal oxidation forms an insulating film, this insulating film being a gate insulating film of an insulated gate field effect transistor (see claim 2); and/or wherein thickness of the gate insulating film is not more than 5 nm, with a gate

length thereof of not more than 0.25 μm (see claim 3); and/or wherein the thickness of the gate insulating film is not more than 3 nm (see claim 4); and/or temperatures (a) of forming moisture with use of a catalyst, transferred into the vertical wafer heat treatment chamber to form the wet oxidative atmosphere, and (b) at which the thermal oxidation is performed, as in claim 5; and/or wherein the thermal oxidation is performed while providing the heat treatment chamber with the wet oxidative atmosphere (see claim 6); and/or additional processing steps prior to transfer of moisture into the vertical wafer heat treatment chamber and after the thermal oxidation, as set forth in claims 7 and 8.

The present invention is directed to a method of fabricating a semiconductor integrated circuit device, particularly useful for formation of gate insulating films such as gate oxide films of metal oxide semiconductor field effect transistors. According to the present invention, moisture, for thermal oxidation, is prepared at a first (relatively low) temperature by use of a catalyst, and through passage of the moisture through a gas introducing tube disposed along a wall surface of the vertical wafer heat treatment chamber from its lower end to its upper end with gas being introduced at the upper end of the vertical wafer heat treatment chamber, the wet oxidative atmosphere can be heated prior to introduction into the vertical wafer heat treatment chamber by passing along a wall surface of the vertical wafer heat treatment chamber, as can be seen in Fig. 30. Thus, the prepared moisture is effectively and efficiently heated, prior to its introduction into the batch processing vertical oxidation furnace, and forms a stable flow downwards in the heat treatment chamber. In addition, with the gas introducing tube being integrally formed with the wall surface of the vertical wafer heat treatment chamber on the wall surface of this heat treatment chamber, efficient heat transfer is achieved, and without any

problems with respect to weaknesses in the gas introducing tube (that is, a strong structure, to, e.g., withstand periodic high temperature heat treatment in mass production, is achieved). Furthermore, since both gas supply and outlet structures are through the lower end of the vertical wafer heat treatment chamber, maintenance time will be reduced, and thermal and mechanical endurance will be greatly improved, the structure having both gas supply and outlet through the lower end of the chamber being much simpler as compared, for example, where gas entry is at the upper end portion of the chamber.

In addition, through use of the vertical oxidation furnace having the vertical wafer heat treatment chamber, a furnace of relatively large capacity is utilized to thereby increase production in connection therewith.

Ohmi discloses apparatus for forming low-temperature oxide films, capable of forming highly pure oxide films at low temperatures when forming oxide films on substrates in semiconductor manufacturing processes or the like. The apparatus includes an oxidation furnace possessing a gas supply port and a gas exhaust port, a heater for heating the oxidation furnace to an arbitrary temperature, and a gas supply system disposed upstream of the oxidation furnace and provided with a mechanism for adding an arbitrary quantity of water or a mechanism for generating an arbitrary quantity of water. See column 2, lines 8-17. Note also column 2, lines 34-40. In one embodiment seen in Fig. 1, water vapor is generated by dissociation of hydrogen by catalytic action of stainless steel pipe 1103a and heating the piping to a temperature within a range of 200°-600°C, and this generated water vapor is supplied, in the form of, e.g., a mixed gas with oxygen, from gas introduction port 1105 to oxidation furnace 1101. The gas is passed to gas exhaust port 1106. Note, for example, from column 2, line 64 to column 3, line 23, together with Fig. 1.

Initially, as can be seen, for example, in Fig. 1, the oxidation furnace 1101 is a horizontal furnace. Moreover, in this furnace gas is supplied to one end thereof, flows through the furnace and outlets from the other end thereof. It is respectfully submitted that this reference would have neither taught nor would have suggested, and in fact would have taught away from, the vertical wafer heat treatment chamber as in the present claims, or wherein the wet oxidative atmosphere is introduced into the heat treatment chamber through the gas introducing tube disposed along a wall surface of the heat treatment chamber from its lower end to upper end, the gas introducing tube having its outlet at the upper end of the vertical wafer heat treatment chamber so that the wet oxidative atmosphere flows from the upper end to the lower end in the vertical heat treatment chamber, and advantages thereof as discussed in the foregoing; and/or the other features of the present invention as discussed in the foregoing, including wherein the gas introducing tube is integrally formed with the wall surface of the vertical wafer heat treatment chamber, and advantages thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

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October 17, 2005

Applicants request any shortage of fees due in connection with the filing of this paper be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 1374.37465C10), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

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Attachment: Modern Semiconductor Device Physics, Edited by S. M. Sze (1998) (5 pp.)

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2 Compound-Semiconductor Field-Effect Transistors

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2.1 INTRODUCTION

2.1.1 Principle of FET Operation

The concept of the field-effect transistor (FET) was first proposed as early as the 1930s by Lilienfeld and Heil.[1] But only in the 1950s had semiconductor–material processing technology progressed far enough that Dacey and Ross were able to demonstrate working devices.[2] In the early 1960s, this technology started to displace bipolar junction transistors.

Currently, FET technology plays a dominant role in electronics, and FET devices and integrated circuits are made in a variety of designs and with many different semiconductor materials. Today, most FETs are made from silicon, because of this material's many excellent properties. However, compound-semiconductor FETs, considered in this chapter, occupy respectable niches, especially in high-speed, high-frequency applications, as well as in electronics that has to withstand harsh environments, including high and low temperatures and exposure to high-energy radiation. As a measure of the maturity of compound-semiconductor FET technology, we note that the integration level of GaAs digital circuits has reached more than one million FETs on a chip.

Figure 1a shows the basic structure of a GaAs metal–semiconductor

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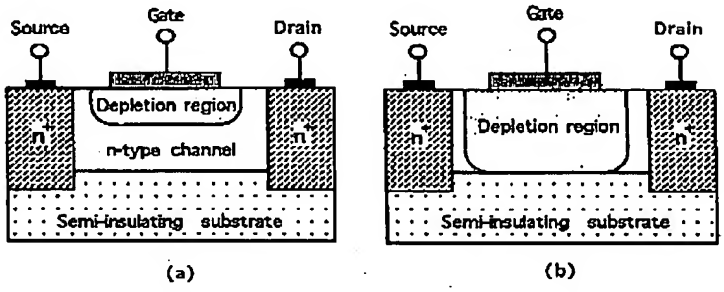

Fig. 1 Schematic MESFET structure at zero drain bias above threshold (a) and below threshold (b).

field-effect transistor (MESFET), which is the most important compound-semiconductor FET. Typically, the GaAs MESFET consists of a semi-insulating or p-type substrate supporting a thin n-type conducting GaAs layer to which three contacts are attached—the ohmic source and drain contacts, and the Schottky gate contact. The conducting layer between source and drain constitutes the FET channel, whose resistance is modulated by the voltage V_{gs} applied between gate and source.* As indicated in Fig. 1b, the rectifying metal–semiconductor gate contact creates a depletion region in the MESFET channel, whose thickness depends on V_{gs}.

When the gate bias is sufficiently negative, the channel is fully depleted (depletion-mode device) and the current between the source and drain becomes very small. The gate–source voltage at which this occurs is called the threshold voltage V_T. Above threshold, the incremental variation of depletion charge per unit area, ΔQ_d, is roughly proportional to the gate voltage variation, ΔV_{gs}:

$$\Delta Q_d = C\Delta V_{gs} \tag{1}$$

where $C = \varepsilon_s/h$ is the differential gate–channel capacitance per unit area, ε_s is the dielectric permittivity of the semiconductor material and h is the thickness of the depletion region. Also, we have $\Delta Q_d = -q\,\Delta n_s$ where n_s is the concentration of conduction electrons per unit area in the channel and q is the unit charge.

This basic principle of the capacitive charge modulation of the conductive channel is common to all FETs. Different FETs use different variations of this principle. They differ by where the channel charge is located, how the isolation between the gate and the channel is achieved, and what materials

*V_{gs} is the extrinsic gate–source voltage, which is larger than the intrinsic gate–source voltage V_{GS} to be discussed later.

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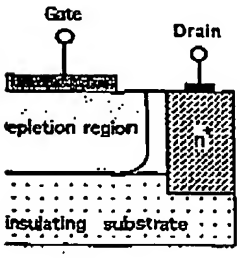

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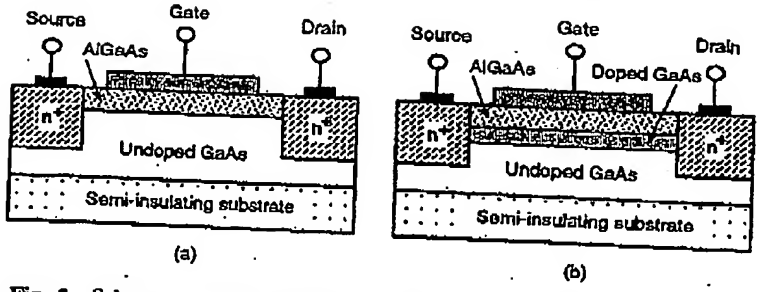

Fig. 2 Schematic structures of (a) HFET and (b) doped-channel HFET.

and doping profiles are used for the gate insulator, the channel, and the substrate.

2.1.2 Types of FETs

In a metal–oxide–semiconductor field-effect transistor (MOSFET), the channel conduction above threshold occurs at the interface of the silicon and the silicon dioxide gate insulator. This device, the most important solid-state device by far, is discussed in Chapter 3.

Heterostructure field-effect transistors (HFETs) are in many ways similar to MOSFETs. In these devices, the gate is separated from the channel by a wide-bandgap semiconductor layer as shown in Fig. 2a, and the channel conduction occurs at the heterointerface.

The MESFET and HFET technologies can be combined in the doped-channel HFET (DCHFET) shown in Fig. 2b. Since compound semiconductors lack good native oxides (such as SiO_2 for Si), MESFETs and HFETs are the devices of choice for compound-semiconductor FETs.

2.1.3 Basic Material Properties

Compound-semiconductor technology is more difficult and is less developed than silicon technology. However, GaAs and several other compound semiconductors have certain advantages over silicon that for many applications outweigh the disadvantages. The advantages include a direct energy gap and, hence, superior optoelectronic properties, a high low-field electron mobility that contributes to smaller parasitic resistances and a higher device speed, a high peak velocity that leads to higher speed and operating frequencies in short-channel devices, and the availability of semi-insulating substrates that make GaAs well suited for microwave and millimeter-wave monolithic integrated circuits. The disadvantages of GaAs compared to